## REMARKS

Applicant thanks the Examiner for his analysis of the application. For the Examiner's convenience and reference, Applicant's remarks are presented in the order in which the corresponding issues were raised in the Office Action. The distinctions identified and discussed below are presented solely by way of example to illustrate some of the differences between the claimed invention and the cited references. Applicant invites the Examiner to review any references discussed below to ensure that Applicant's understanding of the references is consistent with the Examiner's understanding.

STATUS OF THE CLAIMS

Claims 1-13 remain in the case. Claims 4 and 5 stand objected to. Claims 1-3 and 6-13 stand rejected under 35 U.S.C. § 102(b). Claims 1, 3, 5, 8, 9, 10, 12, and 13 have been amended. Claims 4 and 11 have been canceled. No new claims have been added.

RESPONSE TO CLAIM REJECTIONS UNDER 35 U.S.C. § 102(b)

Claims 1-3, 6-10, 12-13 stand rejected under 35 USC 102(b) as anticipated by U.S. Patent No. 6,161,187 to Mason et al. (hereinafter Mason).

It is well settled that under 35 U.S.C. §102 "an invention is anticipated if . . . all the claim limitations [are] shown in a single art prior art reference. Every element of the claimed invention must be literally present, arranged as in the claim. The identical invention must be shown in as complete detail as is contained in the patent claim." *Richardson v. Suzuki Motor Co., Ltd.*, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). To be anticipated "every element of the claimed invention must be identically shown in a single reference." *In re Bond*, 910 F.2d 831, 15 USPQ 2d 1566 (Fed. Cir. 1990).

Mason teaches an apparatus and method for decreasing power consumption in a computer system by skipping and storing clock interrupts during system inactivity, presenting the interrupts to the CPU after reception of a non-interval interrupt or other event.

Claim 1 has been amended to include the limitations of Claim 4, which the Examiner has indicated as containing allowable subject matter. Applicants therefore submit that Claim 1 and its dependents are allowable.

In the Office Action of 21 September 2006, the Examiner did not specifically address or respond to Applicants' previous arguments and amendments with regard to Claim 1's dependent claims, other than to repeat the statements made in the previous Office Action of 20 April 2006. Applicants reassert those arguments with regard to those claims. In addition, independent claims 8, 9, 10, 12, and 13 have been amended to include limitations from one or more of those dependent claims; Applicants reassert their previous arguments with regard to their corresponding amendments.

Claim 8 has been amended to include the limitations of Claim 2, as applied to frequency rather than voltage. Mason teaches the de-assertion of a CPU_PWR_EN signal which, in its absence, stops the CPU from executing instructions "in order to place it in a low-power consuming mode." Col. 3, lines 45-48. Amended Claim 8, in contrast, is limited to the execution and sending of a positive halt-grant instruction and signal which allows the instruction execution module to halt, this action occurring only after execution of the frequency reduction instruction. Mason does not teach the halt grant signal, nor does he teach the sequence of instruction execution claimed in Claim 8.

Additionally, Mason does not teach a low-frequency operating mode, as claimed, but, rather, only a low-frequency halt mode.

Claim 9 has been amended to include the limitations of Claim 3. Mason teaches placing the CPU in a low-power consuming mode, storing interval interrupt assertions, with the CPU remaining in that mode until assertion of a non-interval clock interrupt or other event, at which time the CPU regains normal operating voltage and receives the stored interrupt assertions. Col. 8, line 60-col. 9, line 9.

Amended Claim 9 is limited to the mode controlling module taking the CPU out of low-voltage halt mode and placing it in low-voltage operation mode in response to an interrupt request, only subsequently changing to normal voltage operating mode. In contrast, Mason teaches placement of the CPU directly into normal operating mode upon reception of an interrupt. Mason does remain in low-voltage mode during interval clock interrupts, but those interrupts are stored by an interface chipset, not received by the CPU as claimed in Claim 3.

Claim 10 has been amended to include the limitations of Claim 6, as applied to frequency rather than voltage. Mason teaches placing the CPU in a low-power consuming mode in which the voltage is either zero or a value greater than zero. The Examiner continues to maintain that the zero

voltage can be considered as Applicants' Claim 10 (Claim 6) voltage reduction mode, with the non-zero voltage being equivalent to the low-voltage operation mode. Both claims 10 and 6 have been amended to make clear that the voltage reduction mode is a non-zero voltage state.

Claim 12 has been amended to include the limitations of Claim 7, as applied in method form. The Examiner maintains that Mason's non-zero reduced voltage may be viewed as the intermediate-voltage operation mode of Claim 7 (12). With regard to Claim 7 (12)'s low-voltage operation mode, however, the only statement from the Examiner is that Mason's non-zero reduced voltage can also be viewed as the low-voltage operation mode. That would make Claim 7 (12)'s intermediate-voltage operation mode the same as the low-voltage operation mode, contrary to the language of Claim 7 (12) which plainly differentiates their voltage levels. Additionally (though the Examiner did not address this specifically) it would be impossible to view Mason's zero-voltage level as the low-voltage operation mode of Claim 7 (12), since there must be some voltage in the low-voltage operation mode in order to enable the halting of the instruction execution module (Claim 1).

Applicant additionally notes that Mason teaches placing the CPU in *either* the zero *or* non-zero state. Col. 5, lines 50-60. Claim 7's limitations (with equivalent limitations in Claim 12) include: "said voltage controlling module operates said central processing unit and places said central processing unit into an intermediate-voltage operation mode in which the operating voltage is lower than the operating voltage in said normal mode and higher than the operating voltage in said low-voltage operation mode and *then* places said central processing unit into said low-voltage operation mode" (emphasis added), clearly limiting the claim to placing the CPU in one mode and then the other, not either one alternatively as taught by Mason.

Claim 13 has been amended to include the limitations of Claim 4, as applied in method form. Since the Examiner has indicated allowability of subject matter in Claim 4, Applicants submit that amended Claim 13 is allowable.

ALLOWABLE SUBJECT MATTER

The Examiner indicated allowable subject matter in Claims 4 and 5, but objected to them as depending on a rejected base claim (Claims 3 and 4). Claim 4 has been incorporated into independent claims 1 and 13, and Claim 5 has been amended to depend from Claim 1.

If any impediments to the prompt allowance of the claims can be resolved by a telephone conversation, the Examiner is invited to contact the undersigned.

Respectfully submitted,

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